ABSTRACT

The invention recasts the virtual register file frame calls to alias hazard detection in the hazard detect logic of the physical register file. By way of example, mapping to the stacked registers may be aliased with three sets of 32 registers rows, from 32 to 127, for data hazard calculations to decrease size implementation with minor performance decrease. The invention sacrifices occasional hazard detections – resulting in occasional pipeline stalls as a loss of processor performance - in order to remove the row-by-row dependencies on physical register size. The invention thus reduces the logic requirements associated with the "height" and "width" of the register file: "height" corresponds to the number of registers (e.g., 128), and "width" corresponds to the pipeline stages. The physical register size of the invention is effectively greater than what may be accessed by software at any time; there is no longer a one-to-one correspondence between the virtual and physical register files. In addition, there is no longer a one-to-one correspondence between physical registers and register identifiers for data hazard purposes. Accordingly, more physical registers may be added without a corresponding increase in the hazard detect and bypass logic. If a data hazard exists, an occasional pipeline stall may occur that would not have occurred by incorporating a one-to-one mapping between the register identifiers and physical register files. The physical and decode logic is simplified for the multiple rows of the register file, thereby reducing physical size and power requirements for the EPIC processor.